PRELIMINARY

RFLM-143173HC-150

Wei Bo Associates HK Limited

Ku Band High Power Limiter Module: Ultra Low Flat Leakage & Fast Recovery Time

Features:

- Frequency Range: 14.0 to 17.5 GHz
- High Average Power Handling: +46dBm
- Peak Power: +50dBm
- Low Insertion Loss: <1.2dB
- Return Loss: >15 dB
- Low Flat Leakage Power: <14dBm
- Low Spike Energy Leakage: <0.5ergs
- Ultra Fast Recovery Time: < 700 nsec
- Module Dimensions: 9mm x 6mm x 2.5mm
- DC Blocking Capacitors
- "Always On Protection"
    - No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-143173HC-150 SMT Silicon PIN Diode Limiter Module offers "Always On" High Power CW and Peak protection in the Ku Band region. This Limiter Module is based on proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-143173HC-150 offers excellent thermal characteristics in a compact, low profile 9mm x 6mm x 2.5mm package. It is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent Flat and Spike Leakage for effective receiver protection in the Ku Band frequency range.

The RFLM-143173HC-150 Limiter Module provides outstanding passive receiver protection (Always on) which protects against High Average Power up to +46 dBm @ T_{case}=+55^{o}C, High Peak Power up to +50dBm (Peak) Pulse Width = 50 usec, Duty Cycle = 20%, T_{case}= +55^{o}C, maintains low flat leakage to less than 14 dBm (typ), and reduces Spike Leakage to less than 0.5 ergs(typ).

ESD and Moisture Sensitivity Rating

The RFLM-143173HC-150 Limiter Module carries a Class 1C ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The proprietary design methodology minimizes the thermal resistance from the PIN Diode junction to base plate. The two stage limiter design employs a two stage detector circuit which enables ultra-fast turn on of the High

Power PIN Diodes. This circuit topology coupled with the thermal characteristic of the substrate design enables the Limiter Module to reliably handling High Input RF Power up to +46 dBm CW and RF Peak Power levels up to +50 dBm (50uSec pulse width @ 20% duty cycle) with base plate temperature at +55°C.The RFLM-143173HC-150 based substrate has been design to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns.

Absolute Maximum Ratings

@ Z_0=50Ω, T_A= +25°C as measured on the base ground surface of the device unless otherwise noted.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	T = 30 seconds	260°C
RF Peak Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2:1, RF Pulse width = 50 usec, duty cycle = 20%, derated linearly to 0 W at T_{CASE}=150°C (note 1)	+50dBm
RF CW Incident Power	T_{CASE}=+55°C, source and load VSWR < 1.2:1, derated linearly to 0 W at T_{CASE}=150°C (note 1)	+46dBm
RF Input & Output DC Block Capacitor Voltage Breakdown		100 V DC

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

RFLM-143173HC-150 Electrical Specifications

@ Z_o=50Ω, Ta= +55°C as measured on the base ground surface of the device.

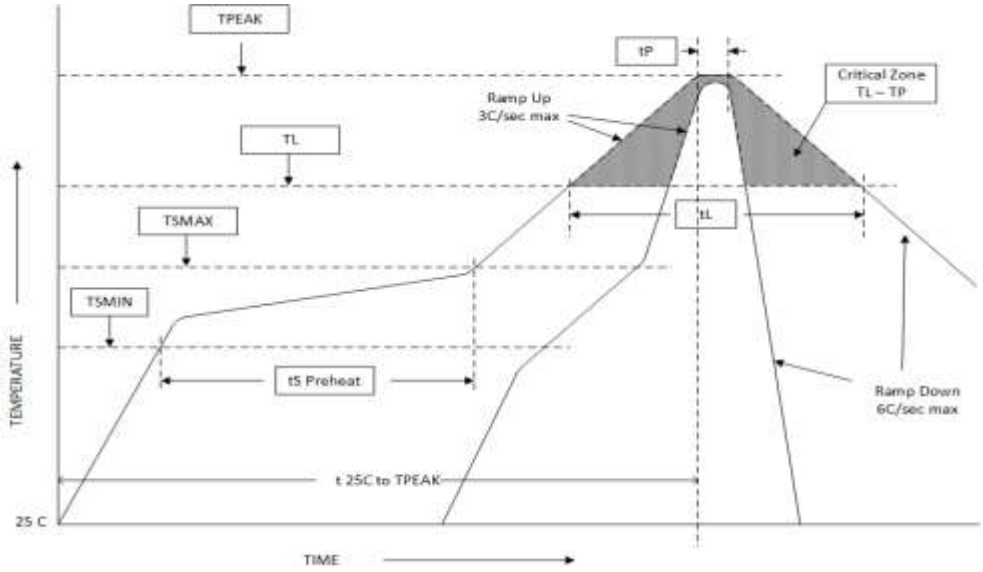
Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F	14.0 GHz ≤ F ≤ 17.5GHz	14.0		17.5	GHz
Insertion Loss	IL	14.0 GHz ≤ F ≤ 17.5 GHz, P_{in}= -20dBm			1.2	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	14.0 GHz ≤ F ≤ 17.5 GHz, Pin ≤ -20 dBm		0.005		dB/°C
Return Loss	RL	14.0 GHz ≤ F ≤ 17.5 GHz, Pin= -20dBm	15			dB
Input 1 dB Compression Point	IP_{1dB}	14.0 GHz ≤ F ≤ 17.5 GHz		5		dBm
2nd Harmonic	$2F_o$	P_{in}= -20 dBm, F_o= 15.0 GHz		-40	-30	dBc
Peak Incident Power	$P_{inc\ (PK)}$	RF Pulse = 50 usec, duty cycle = 20%, t_{rise} ≤ 3us, t_{fall} ≤ 3usec			+50	dBm
CW Incident Power	$P_{inc(CW)}$	14.0 GHz ≤ F ≤ 17.5 GHz T_{case} = +55°C			+46	dBm
Flat Leakage	FL	P_{in} = +50dBm, RF Pulse width = 50 us, duty cycle = 20%, t_{rise}≤ 3 us, t_{fall}≤ 3 us			14	dBm
Spike Leakage	SL	Pin = +50dBm, RF Pulse width = 50 us, duty cycle = 20%			0.5	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, Pin = +50dBm peak, RF PW = 50 us, duty cycle = 20%, trise ≤ 3us, t_{fall} ≤ 3usec			700	nsec

Assembly Instructions

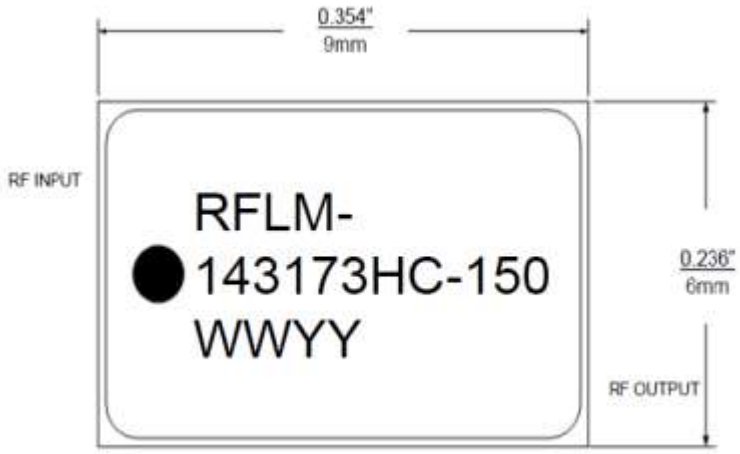
The RFLM-143173HC-150may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

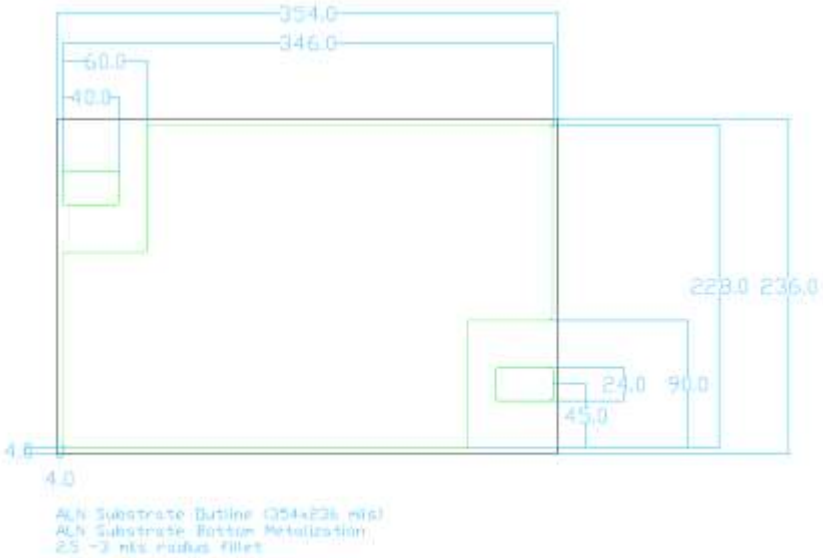
Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat Temp Min (T_{smin}) Temp Max (T_{smax}) Time (min to max) (t_s)	 100°C 150°C 60 – 120 sec	 100°C 150°C 60 – 180 sec
T_{smax} to T_L Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	260°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above: Temp (T_L) Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



RFLM-143173HC-150 Limiter Module Foot Print Drawing





Notes:

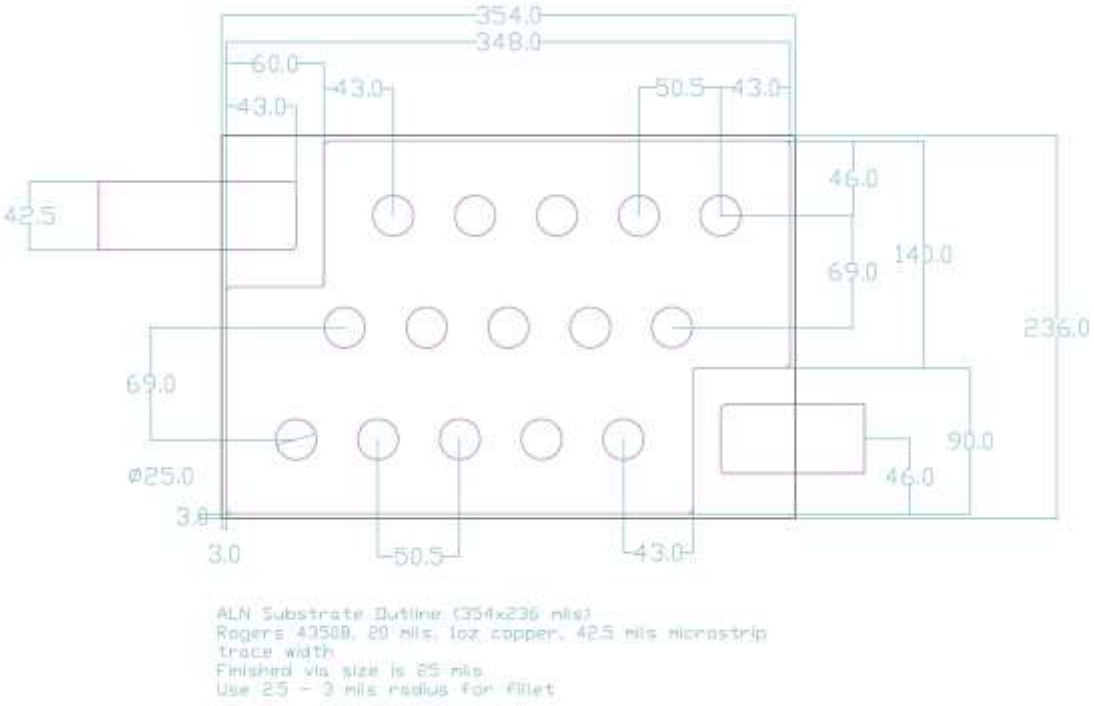
1) Plain surface is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
2) Back side metallization is thin Au termination plating to combat Au embrittlement (Au plated over Cu).
3) Unit = mils

Thermal Design Considerations:

The design of the RFLM-143173HC-150 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than +55 ^{o}C.

There must be a minimal thermal and electrical resistance between the limiter module and ground. Adequate thermal management is required to maintain a T_{jc} at less than +175°C and thereby avoid adversely affectingthe semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shade in red in the figure shown below.

Recommended RF Circuit Solder Footprint for the RFLM-143173HC-150



Notes:

1) Recommended PCB material is Rogers 4350B, 20 mils thick (RF Input and Output trace width needs to be adjusted from the recommended footprint.)
2) Plain surface is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.
3) Unit = mils

Part Number Ordering Detail:

The RFLM-143173HC-150 Limiter Module is available in the following format:

Part Number	Description	Packaging
RFLM-143173HC-150	Ku Band Limiter with Internal Input & Output DC Blocking Capacitprs	Gel-Pack